REMARKS

Claims 1-8, 14-16, 21-22, and 26-27 are pending. The Office Action dated August 21, 2006, in this Application has been carefully considered. The above amendments and the following remarks are presented in a sincere attempt to place this Application in condition for allowance. Claims 1-8, 14-16, and 21-22 have been amended, and claims 26-27 added, in this Response. Claims 9-13, 17-20, and 23-25 have been cancelled in this Response. Reconsideration and allowance are respectfully requested in light of the above amendments and the following remarks.

Claims 2, 3, 22, and 23 were objected to due to informalities. Specifically, the Examiner stated it would be more appropriate to replace "where" with "wherein". In response thereto, Applicant has amended claims 2, 3, and 22 to replace "where" with "wherein". Applicant notes claim 23 is canceled herein.

Claim 24 was rejected under 35 U.S.C. 101 as being directed to non-statutory subject matter. In response thereto, Applicant notes claim 24 is canceled herein.

Claims 1-14, 17, and 23 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. In response thereto, Applicant notes that claims 1-8 and 14 are amended herein and no longer contain the objectionable language cited in the Office Action. Applicant notes claims 9-13, 17, and 23 are canceled herein.

Claims 14, 15, 17, 21, 22, 24, and 25 were rejected under 35 U.S.C. 103(a) as being unpatentable over Patterson and Hennessey [Computer Architecture: A Quantitative Approach] (hereinafter "Patterson") and Williams et al. [U.S. 6,693,630 B1] (hereinafter "Williams"). Applicant respectfully traverses this rejection as it applies to claims 14-15 and 21-22, and notes claims 17 and 24-25 are canceled herein.

The combination of Patterson and Williams does not teach or disclose a method for providing memory data to a requestor of the memory data, the method including: requesting a memory block from a memory hierarchy level having a coherence directory, associated coherence directory data, and a plurality of prefetch address registers; ***generating a response including the memory data and corresponding coherence directory data***; updating the directory coherence data corresponding to the memory data and indicating the address of a prefetched block in a prefetch address register; ***receiving the response including the memory data and the corresponding coherence directory data from said memory hierarchy level***; determining whether the received coherence directory data is compatible with a required access mode; performing at least one coherence action if the received coherence directory data is incompatible with the required access mode; and providing the memory data to the requestor of the memory data.

As amended herein, claim 14 recites (emphasis added):

14. A method for providing memory data to a requestor of the memory data, the method comprising:

requesting a memory block from a memory hierarchy level having a coherence directory, associated coherence directory data, and a plurality of prefetch address registers;

generating a response including the memory data and corresponding coherence directory data;

updating the directory coherence data corresponding to the memory data and indicating the address of a prefetched block in a prefetch address register;

receiving the response including the memory data and the corresponding coherence directory data from said memory hierarchy level;

determining whether the received coherence directory data is compatible with a required access mode;

performing at least one coherence action if the received coherence directory data is incompatible with the required access mode; and

providing the memory data to the requestor of the memory data.

Claim 14 recites "generating a response including the memory data and corresponding coherence directory data." In the Office Action, the Examiner points to "...messages sent among nodes to maintain coherence, see page 681 and Fig. 8.23 [of Patterson]..." Patterson is a computer architecture textbook that generally describes directory-based cache-coherence protocols. Applicant asserts that Patterson does not teach or suggest "generating a response including memory data and corresponding coherence directory data." None of the messages sent among nodes to maintain coherence described by Patterson on page 681 and in Fig. 8.23 include "memory data and corresponding coherence directory data" as recited in claim 14.

The Williams patent discloses a data pre-fetch system for a cache memory wherein a second-level cache includes pre-fetch control logic 304 (Fig. 3) coupled to a general register array (GRA) 300 (Fig. 3). The pre-fetch control logic 304 controls the storing of requests in the GRA 300, performs pre-fetch processing on the requests stored in the GRA 300, and provides requests to logic that determines whether a requested address is resident within cache memory. If the requested address is not resident within the cache memory, a pre-fetch request is generated to obtain the cache line. (Williams, col. 10, lines 4-34). Applicant asserts that Williams does not describe "generating a response including the memory data and corresponding coherence directory data" as recited in clime 14.

Claim 14 also recites "receiving a response including the memory data and the corresponding coherence directory data from said memory hierarchy level." In the Office Action, the Examiner again points to "...messages sent among nodes to maintain coherence, see page 681 and Fig. 8.23 [of Patterson]..." Applicant asserts that Patterson does not teach or suggest "receiving

a response including the memory data and the corresponding coherence directory data from said memory hierarchy level." None of the messages sent among nodes to maintain coherence described by Patterson on page 681 and in Fig. 8.23 include "memory data and the corresponding coherence directory data from said memory hierarchy level" as recited in claim 14. Applicant also asserts that Williams does not describe "receiving a response including the memory data and the corresponding coherence directory data from said memory hierarchy level" as recited in claim 14.

For at least the above reasons, Applicant asserts the combination of Patterson and Williams fails to teach or disclose all of the elements and limitations of pending independent claim 14. Applicant also believes that pending claims 15-16 and 21-22 that depend from claim 14 are also allowable for at least the above reasons.

In the present response, Applicant addresses all of the claim objections and rejections cited in the Office Action. In view of the amendments to the claims and Applicant's remarks, Applicant believes pending claims 1-8, 14-16, 21-22, and 26-27 are in condition for allowance, and respectfully request allowance of pending claims 1-8, 14-16, 21-22, and 26-27.

With the amendments to the claims presented herein, there are currently 3 pending independent claims and 15 total pending claims in the application. As the original application had 4 independent claims and 25 total claims, Applicant believes no additional fees are due. In the event that any other fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of CARR LLP.

The present amendment is believed to contain a complete response to the issues raised in the Office Action. Full reconsideration is respectfully requested. If the Examiner should have any questions, comments or suggestions, the undersigned attorney earnestly requests a telephone

conference. In particular, should the Examiner deem that any further amendment is desirable to place this application in condition for allowance, the Examiner is also invited to telephone the undersigned at the number listed below.

Respectfully submitted,

CARR LLP

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